EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jon Harris on 06/09/2010.

The application has been amended as follows:

In the claims:

Claims 2, 4, 9, 21 and 33 are canceled.

1. (Currently Amended) A system comprising:

a first node that broadcasts a request for data; and

a second node having a first state associated with the data that defines the second node as an ordering point for the data, the second node providing a response to the first node that transfers the ordering point to the first node in response to the request for the data;

wherein the second node transitions from the first state to a transition state associated with migration of the ordering point to the first node;

wherein the first node transitions to a second state associated with the data in response to receiving the response from the second node, the second state defining the first node as the ordering point for the data;

wherein the first node comprises a processor having an associated cache that comprises a plurality of cache lines, one of the cache lines having an address associated with the data, the second state identifying the one of the cache lines as the ordering point for the data in the system; and

wherein the first node provides an acknowledgment signal to the second node after receiving responses from other nodes in the system.

3. (Currently Amended) The system of claim ~~2~~1, wherein the second state corresponds to a state of a cache line that contains the data, the second state enabling the first node to provide an ownership data response that includes a copy of the data to requests for the data.

10. (Currently Amended) The system of claim ~~9~~1, wherein the second node provides a signal to the first node indicating receipt of the acknowledgement signal.

13. (Currently Amended) The system of claim 1, wherein each ~~of the first and second nodes comprises a processor having an associated cache that comprises a plurality of cache lines, each~~ cache line ~~having~~ has a respective address that identifies associated data and state information that identifies a state of the associated data for the respective cache line, each of the processors being capable of communicating with each other via an interconnect.

15. (Currently Amended) A computer system, comprising:

a source processor that issues a broadcast request for desired data while having a first state associated with the desired data; and

an owner processor having an associated cache that includes the desired data in a cache line, the cache line having an associated state that defines a copy of the desired data as an ordering point for the desired data, the owner processor responding to the broadcast request with an ownership data response that includes the desired data, the source processor transitioning from the first state to a second state associated with the desired data based on the ownership data response, the second state defining the source processor as the ordering point for the desired data;

wherein the source processor provides an acknowledgment signal to the owner processor after receiving a complete set of responses from the system, the acknowledgement signal enabling the owner processor to transition from a transition state to an invalid state.

22. (Currently Amended) The system of claim ~~21~~15, wherein the owner processor provides a signal to the source processor indicating receipt of the acknowledgement signal.

24. (Currently Amended) A system, comprising:

means for broadcasting a request for data from a first processor node having a cache state associated with the requested data;

means for providing an ownership data response from a second processor node having a cache state that defines the second processor as a cache ordering point for the requested data;

means for transferring the cache ordering point from the second processor node to the first processor node associated with the first processor node receiving the ownership data response from the second processor node; ~~and~~

means for reissuing a request in the system using a forward progress protocol in response to detecting a conflict while employing a source broadcast protocol in each of the means for broadcasting, the means for providing and the means for transferring; and

means for providing a migration acknowledgment signal to acknowledge receipt of the ownership data response at the first processor node and for transitioning to a cache state at the first processor node that defines the first processor node as the cache ordering point; and

wherein the first node comprises a processor node that includes a cache having a plurality of cache lines, one of the cache lines of the processor node having a state associated with the requested data, the state associated with the one of the cache lines defining the first node as the new cache ordering point.

28. (Currently Amended) A method comprising:

broadcasting from a source node a request for requested data;

providing an ownership data response from an owner node in response to the request from the source node;

transitioning a state at the source node associated with the requested data from a first state to a second state in response to receiving the ownership data

response, the second state defining the source node as a new cache ordering point;

providing a migration acknowledgment signal from the source node to acknowledge receipt of the ownership data response at the source node;

entering a transition state at the owner node in response to providing the ownership data response; and

releasing the owner node from the transition state in response to the migration acknowledgment signal;

wherein the source node comprises a processor node that includes a cache having a plurality of cache lines, one of the cache lines of the processor node containing the requested data based on the ownership data response and having a state associated therewith, the state associated with the one of the cache lines defining the source node as the new cache ordering point.

REASONS FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance:

Independent claims 1, 15, 24 and 28 among other things teach:

A first node that broadcasts a request for data and a second node having a first state associated with the data that defines the second node as an ordering point for the data, the second node providing a response to the first node that transfers the ordering point to the first node in response to the request for the data and wherein the second node transitions from the first state to a transition state associated with migration of the ordering point to the first node and wherein the first node transitions to a second state associated with the data in response to receiving the response from the second node, the second state defining the first node as the ordering point for the data and wherein the first node comprises a processor having an associated cache that comprises a plurality of cache lines, one of the cache lines having an address associated with the data, the second state identifying the one of the cache lines as the ordering point for the data in the system and wherein the first node provides an acknowledgment signal to the second node after receiving responses from other nodes in the system.

The system provides for a coherency protocol that facilitates migration of an ordering point for data. The coherency protocol can enable ordering point migration while a broadcast-based protocol continues to run and process requests and responses associated with data. The state of the data stored in the cache can define the ordering point associated with the data, which can be transferred from one cache to another wherein the first node comprises a processor having an associated cache that

comprises a plurality of cache lines, one of the cache lines having an address associated with the data, the second state identifying the one of the cache lines as the ordering point for the data in the system.

The prior art does not teach the cited limitation.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CORRESPONDANCE INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FARHAD ALI whose telephone number is (571)270-1920. The examiner can normally be reached on Monday thru Friday, 7:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey C. Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Farhad Ali/
Examiner, Art Unit 2446

/Benjamin R Bruckart/
Primary Examiner, Art Unit 2446